AMENDMENTS TO THE CLAIMS

1-35. (Cancelled)

36. (New) A sensing circuit for sensing a resistance value of a first resistive element in a memory device, the circuit comprising:

a first capacitor and at least one reference capacitor;

a charging circuit for charging said first and said at least one reference capacitors to a predetermined voltage value;

at least one reference resistive element;

a first discharge circuit for discharging said first capacitor through the first resistive element, said first discharge circuit having a first discharge characteristic;

a second discharge circuit for discharging said at least one reference capacitor through said reference resistive element, said second discharge circuit having a second discharge characteristic; and

a comparison circuit for comparing said first discharge characteristic to said second discharge characteristic.

37. (New) The sensing circuit of claim 36 wherein said first and second discharge characteristics are voltage levels.

38. (New) The sensing circuit of claim 37 wherein said at least one reference capacitor comprises first and second reference capacitors and said at least one reference resistive element comprises first and second resistive elements respectively associated with said first and second reference capacitors, wherein said first reference capacitor

discharges through said first reference resistive element and said second reference capacitor discharges through said second reference resistive element.

39. (New) The sensing circuit of claim 38 wherein said first and second reference resistive elements respectively have resistance values corresponding to a binary "1" value and a binary "0" value.

40. (New) The sensing circuit of claim 36 further comprising a regulation circuit for maintaining a predetermined voltage across said selected resistive element during discharge of said capacitors.

41. (New) The sensing circuit of claim 40 wherein said regulation circuit comprises a voltage source and a switch for selectively connecting said voltage circuit to said capacitors.

42. (New) A resistive memory sensing apparatus comprising:

means for applying an electrical charge to a plurality of storing means;

first discharge means for discharging a first stored electrical charge through a first resistive element according to a first, measurable discharge characteristic, said first resistive element having one of a first or a second programmed resistance;

second discharge means for discharging a second stored electrical charge through a reference resistive element, said second discharge means discharging according to a second, predictable discharge characteristic; and

means for comparing said first and said second discharge characteristics and for outputting a result based on said comparison.

43. (New) The resistive memory sensing apparatus of claim 42 wherein the first and second discharge characteristics comprise a rate of decaying voltage on said first and second discharge means respectively.

44. (New) The resistive memory sensing apparatus of claim 42 wherein said first and second programmed resistances are resistive values corresponding to a binary logic value of "1" and a logic value of "0" respectively.

45. (New) The resistive memory sensing apparatus of claim 44 wherein said reference resistive element has a reference resistance value of between a value corresponding to a logical "1" and a value corresponding to a logical "0."

46. (New) The resistive memory sensing apparatus of claim 42 wherein said second discharge means comprises first and second reference capacitive structures, and said reference resistive element comprises first and second reference resistance elements corresponding to and associated with a respective one of said first and second reference capacitive structures.

47. (New) The resistive memory sensing apparatus of claim 46 wherein said first reference resistance element has a resistance value approximately equal to a value corresponding to a logical "1" value and wherein said second reference resistance element has a resistance value approximately equal to a value corresponding to a logical "0" value.

48. (New) The resistive memory sensing apparatus of claim 42 further comprising a switch means for selectively connecting said applying means to selective ones of said plurality of storing means.

49. (New) A method for converting a resistance into a logic state signal, said method comprising:

charging a first capacitor and at least one reference capacitor;

discharging the first capacitor through a first resistance element;

discharging the at least one reference capacitor through at least one reference resistance element;

sensing a first discharge characteristic of said first capacitor and a second discharge characteristic of said at least one reference capacitor;

comparing said first and second discharge characteristics; and

outputting a logic signal based on said comparison.

50. (New) The method of claim 49 wherein said charging steps comprise connecting each capacitor to a common voltage source having a predetermined voltage level.

51. (New) The method of claim 49 wherein said step of sensing a first and second discharge characteristic comprises taking a quantitative measurement of at least one of voltage and current.

52. (New) The method of claim 49 wherein said sensing said second discharge characteristic of said at least one reference capacitor comprises sensing a discharge characteristic of a first reference capacitor and sensing a discharge characteristic of a second reference capacitor and averaging said discharge characteristics.

53. (New) A method of reading a logic state from a resistance memory device comprising:

connecting a first resistance element to a first capacitive element to form a resistance memory device;

connecting said resistance memory device to a reference circuit, said reference circuit comprising at least one second capacitive element connected to at least one second resistance element, said second resistance element having a known resistance value;

charging said first and at least one second capacitive elements to a predetermined state;

simultaneously discharging said first and at least second capacitive elements respectively through said first and at least one second resistance elements;

quantitatively measuring a discharge characteristic from each capacitive element;

comparing said quantitative measurements from said first and said at least one second capacitive elements; and

outputting a value representing said comparison.

54. (New) The method of claim 53 wherein said step of charging said first and at least one second capacitive elements comprises applying a reference voltage to each capacitive element.

55. (New) The method of claim 53 wherein said step of quantitatively measuring a discharge characteristic comprises measuring a rate of voltage decay at each of said first and at least one second capacitive elements.

56. (New) The method of claim 53 wherein said step of comparing said quantitative measurements from said first and said at least one second capacitive elements comprises inputting an output of said first resistance element and an output of said reference circuit into a comparator.